An Efficient Testing Methodology for Embedded Flash Memories

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Abstract

The market share of portable and IoT (Internet of Things) devices has been rapidly growing over the last decade. In parallel the amount of non-volatile memories, especially flash memories, used in such devices has also increased significantly due to their low power consumption and capability of in-field programmability. Therefore, for achieving high production yield the reliability and testability of embedded flash memories is considered as a primary requirement. The conventional March tests that are used for random access memories (RAMs) are not appropriate for testing flash memories, since test operations and requirements in flash memories differ from that in RAMs. In this paper, a comprehensive set of flash memory faults are introduced and an efficient methodology is proposed for detection of those faults.

1. Introduction

Flash is a non-volatile memory that is based on floating-gate (FG) concept [1], [2]. It stores data by changing of transistor threshold voltage (Vth), determined by the number of electrons in the FG. The state of the memory cell is represented by charging and discharging the FG using high voltage. There are three main operations for a flash memory: read, program and erase (flash). The read operation reads the data stored in a memory word. Program operation charges the cells of a word. Two types of erase operation exist. First is sector-erase, which discharges all the cells in a sector. The second type is chip erase, that discharges the cells in whole memory.

There are two types of flash memories: NOR flash and NAND flash [2]-[5]. The difference between these types is in their array architecture (see Fig. 1). NOR architecture allows to have read with random access, while in NAND fleshes read access is sequential. On the other hand, the program and erase operations are faster in NAND flashes (see Table 1).

The low-power consumption and the flexibility make flash memories popular for portable and IoT devices. Unfortunately, the evolution of technologies and particularly the flash memory process induces more and more complex faults in such memories.

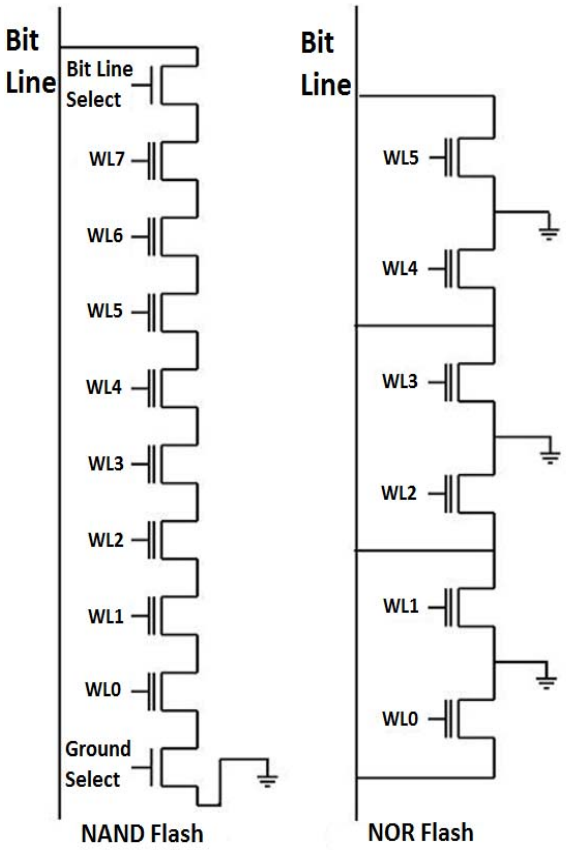

Fig. 1. NAND and NOR Flash Structures

Table 1. Comparison of NAND and NOR Flash Memories

NAND	NOR
Sequential READ access	Random READ access
Fast PROGRAM	Slow PROGRAM
Fast ERASE	Slow ERASE

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Flash memories have no random access for erase operation. They do sector erase or chip erase instead. Therefore, March test algorithms for RAM [6] are not suitable for testing flash memories. In order to test flash memories, extended March like test algorithms [7] are used.

In this paper, we propose an efficient test solution for embedded flash memories with March like test algorithms and background patterns. The paper is organized as follows. Section 2 describes the faults in flash memories. The proposed solution is provided in Section 3. Section 4 concludes the paper.

2. Fault Models

Since flash memories have different cell structures and operations, there are flash specific faults, that do not occur in RAMs.

The reliability issues which occur in floating gate semiconductor arrays are data retention and endurance. Data retention is the ability of flash memory cells to maintain the programmed state for an acceptable period of time. Endurance specifies the number of sequential program-erase cycles that memory sector can handle without disruption. Each program-erase cycle may introduce defects that at some point can prevent from performing successful operations on cells of memory sector. This failure can cause the whole sector to be useless. These two reliability issues need stress test [8].

Besides, disturbance faults can occur in flash memories, that do not correspond to any well-known fault models of RAM memories. These disturbances can have some common characteristics with RAM faults. There are several types of faults common to flash memories [9], [10].

1. Word-line erase disturbance (WED) – The cell becomes erased when another cell on the same word-line is being programmed.
2. Bit-line erase disturbance (BED) – The cell becomes erased when another cell on the same bit line is being programmed.
3. Word-line program disturbance (WPD) - The cell becomes programmed when another cell on the same word-line is being programmed.
4. Bit-line program disturbance (BPD) - The cell becomes programmed when another cell on the same bit-line is being programmed.
5. Source-line program disturbance (SPD) - The cell becomes programmed when another cell on the same source-line is being programmed.
6. Gate read erase disturbance (GRE) - The cell becomes erased, when a read operation is being performed on another cell of the same word-line.
7. Channel read-program disturbance (CRP) – The cell becomes programmed when a read operation is being performed on another cell of the same word-line.
8. Read program disturbance (RPD) – Consecutive read operations on a cell cause it to be programmed.
9. Read erase disturbance (RED) – Consecutive read operations on a cell cause it to be erased.
10. Over erase disturbance (OED)- The erase operation results in decrease of cell threshold voltage and bit-line leakage. The cell cannot be programmed normally. Only after consecutive program operations the cell may be recovered.
11. Over program disturbance (OPD) - The cell is over-programmed and cannot be normally erased. It can be recovered after performing consecutive erase operations.
12. Read disturb (RD: RD0, RD1) - Consecutive read operation on a cell impacts the threshold voltages of affected flash cells and causes them to flip their values.

The RD0, RD1, RPD and RED faults need consecutive read operations to be activated. Since this is just a change in voltage level for certain bits, erasing and reprogramming the affected cells in question completely reverses the effects of these faults.

There are some RAM specific faults, that occur in flash memories also. These common faults are stuck-at faults, transition faults, state coupling faults, address decoder faults, stuck-open faults [6].

3. Testing Methodology

In previous section flash memory faults have been discussed. In this section, we propose a comprehensive set of test mechanisms for flash, including test modes, background patterns and addressing methods.

The flash disturbance faults and common faults with RAMs can be tested using March like test algorithms.

In Table 2, well-known flash test algorithms are described [11]. Each of these algorithms covers a specific set of flash faults. The one that covers wider set of disturbance (except for disturbances that need consecutive read operations) and common faults with RAMs is March-FT algorithm [9].

In this paper, the March-FT algorithm has been extended. A set of testing mechanisms are added to it, in order to perform complete testing of embedded flash memories.

Test operations used in test algorithms are:

a. READ – Performs read operation;
b. PROGRAM – Performs program operation;

Table 2. Well-Known Tes Algorithms

Test Algorithm Name	Description
MSAF	(E); ⇑(R1); ⇑(P); ⇑(R0)
MTF	(E); ⇑(R1); ⇑(P); ⇑(R0); (E); ⇑(R1)
MSOF	(E); ⇑(R1, P, R0)
MAF	(E); ⇑(R1, P, R0); (E); ⇓(R1, P, R0)
MDF	(E); ⇑(R1, P); ⇑(R0); (E); ⇓(R1, P); ⇓(R0)
March-FT	(E); ⇑(R1, P, R0); ⇑(R0); (E); ⇓(R1, P, R0); ⇓(R0)

c. SECTOR_ERASE – Erases the specified sector;
d. CHIP_ERASE – Erases whole memory;
e. DELAY(interval) – No operation is performed within specified interval time.

The proposed types of physical background patterns are the followings:

a. Solid: all 0s (0000…00) or all 1s (1111…11);
b. Checkerboard: odd rows of the memory contain physically 0101…01 data, even rows contain 1010…10 data or vice-versa;
c. Row stripe: odd rows of the memory contain 0000…00, even rows contain 1111…11 or vice-versa;
d. Column stripe: odd columns of the memory contain 0000…00, even columns contain 1111…11 or vice-versa.

There are 4 types of addressing methods in proposed solution:

a. Address increment (0, 1, 2, …, N-1), where N is the number of addresses of a flash memory;
b. Address decrement (N-1, N-2, …, 2, 1, 0);
c. Address complement (0, N-1, 1, N-2, …);
d. Single addressing (no specific address is specified, mainly used with erase operation).

The solution provides availability of predefined test algorithms and test algorithm programmability. It is possible to apply test algorithms to a specified range of flash memories (to main part, redundancy part or other). In order to do fault diagnosis, the support of Stop-On-Nth-Error (SONE) diagnostics mechanism is available. It runs the BIST and stops on the specified Nth fault (by ignoring the detected first N-1 faults) and reports the corresponding diagnostic information of the Nth fault (e.g., logical address of the fault, which March element and which March operation in the test element detected the fault, etc.). As it has been mentioned above, RD, RPD and RED faults need consecutive read operations to be detected. For this purpose, some read operations of original March-FT have been replaced with consecutive reads in extended algorithm. The number of consecutive read operations is user defined. With this change extended algorithm fully covers all disturbance and common faults with RAMs that can occur in embedded flash memories. The proposed algorithm March-FTE (extended March-FT) is the following:

March-FTE:
CHIP_ERASE;
⇑(READ(~D)^n, PROGRAM(D), READ(D)^n);
⇑(READ(D));
CHIP_ERASE;
⇓(READ(~D)^n, PROGRAM(D), READ(D)^n);
⇓(READ(D)).
where:

- D is background pattern – checkerboard, solid, row stripe or column stripe;
- n is the number of loops (how many times the operation should be repeated) - ($n \geq 1$);
- ⇑ - Address increment;
- ⇓ - Address decrement.

Since as already mentioned some of the flash faults need special stress conditions for fault sensitization, the proposed solution provides the following test modes:

a. Apply high voltage for some operations;
b. Bake test for data retention;
c. Address decoding test;
d. Endurance stress.

For data retention testing the March RT test algorithm is proposed, that needs to be run in bake stress mode. The algorithm is following:

March RT:
⇑(PROGRAM(D));
DELAY(interval);
⇑(READ(D)).
where D is background pattern and "interval" is defined by user and specifies the time period during which the cell should be able to stay at programmed state.

For endurance testing consecutive program and erase operations are needed to be performed under endurance stress mode. The MSAF test algorithm from Table 2 is best suited for it. The extended test algorithm MSAF Stress applies to all memory sectors under endurance stress mode.

Table 3 shows the comparison of embedded flash test algorithms. The proposed test algorithms (March-FTE, March RT and MSAF Stress) are in the marked range of the table which together cover all the faults discussed in this paper.

4. Conclusion

The reliability of embedded flash memories is a key issue, since the popularity of these type of non-volatile memories increases rapidly. Because flash memories are based on floating-gate concept, their operations and fault types differ from that of RAMs, therefore the traditional testing methods are not acceptable for flashes. This paper proposes an efficient testing solution for embedded flash memories which provides various mechanisms for performing complete testing. Extended March-like test algorithms, test algorithm programmability, different stress modes and fault diagnosis capabilities are part of the proposed solution.

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Table 3. Fault Coverage of Test Algorithms for Flash Memory Testing

Faults/ Algorithms	WED	BED	WPD	BPD	SPD	GRE	CRP	SAF	TF	CFst	AF	SOF	OED	OPD	RD0	RD1	RPD	RED	Ret.	End.
MSAF	-	-	-	-	-	-	-	+	-	-	-	-	+	-	-	-	-	-	-	-
MTF	-	-	-	-	-	-	-	+	+	-	-	-	+	+	-	-	-	-	-	-
MSOF	-	-	-	-	-	-	-	+	-	-	+	+	+	-	-	-	-	-	-	-
MAF	-	-	-	-	-	-	+	+	+	+	+	+	+	+	-	-	-	-	-	-
MDF	+	+	+	+	+	-	-	+	+	+	+	-	+	+	-	-	-	-	-	-
March-FT	+	+	+	+	+	+	+	+	+	+	+	+	+	+	-	-	-	-	-	-
March-FTE	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	+	-	-
March RT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	+	-
MSAF Stress	-	-	-	-	-	-	-	+	-	-	-	-	+	-	-	-	-	-	-	+