Overview Study on Fault Modeling and Test Methodology Development for FinFET-Based Memories

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Abstract

Rapidly developing FinFET technology, alternative to the conventional planar technology, plays an important role in routing modern silicon industry. Due to unique structure of FinFET transistors the defect types and resulting fault models is different for FinFET transistors compared to planar ones. As a result the well-established flow used for embedded test and repair solutions development for MOSFET-based memories fails to be smoothly deployed for FinFET-based memories as well. Thus there is a need to modify the existing solution to support FinFET-based memories. In the scope of this paper the upgraded test methodology flow is introduced for FinFET-based memories, as well as the high-level overview of the comprehensive study is presented which was conducted using the described flow.

1. Introduction

For many years the considerable market share in embedded semiconductor industry belonged to the memories built with conventional planar MOSFET technology. Nevertheless growing short-channel and current leakage problems of MOSFET transistors make it almost impossible to continue further scaling down of memory cell constructed with this type of transistors without negative consequences. Today it is already proved in practice that MOSFET is no more able to shrink beyond 20nm. This means that the planar technology has reached its full potential and in order to keep up with the Moor's law, there is a need to use the third dimension for constructing the transistors for future System-on-Chips (SoC). Thereby several approaches have been proposed recently among which FinFET technology is considered as having all the necessary preconditions to become the MOSFET successor. The research on FinFET technology has started as early as in 1999 [1] and it began to gradually gain more importance over the time resulting in number of publications ([2]-[4]). Unique structure of FinFET transistors among the other useful features allows significantly reducing short-channel effects making them highly demanded in the modern semiconductor industry.

Fig. 1 shows the 3D structure of FinFETs and displays several of the most important FinFET parameters: height of the Fin (H_{Fin}), its width or body thickness (T_{Fin}), and FinFET channel length (L_g). Due to its structure FinFETs have several advantages including controlled fin body thickness, low threshold-voltage variation and lower operating voltage. Nevertheless it is important to mention that despite the significant power and performance benefits, FinFET design and manufacturing doesn't come at the same cost as MOSFET and is still challenging and costly task [5].

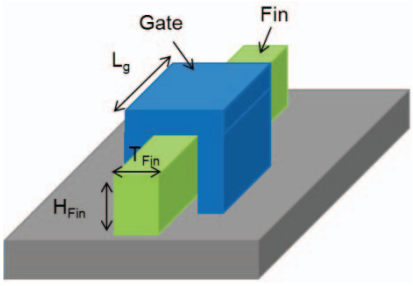

Figure 1. FinFET structure

With the world leading manufacturers coherently announcing the streamline production of FinFET-based memories the problem of test and repair for this type of embedded memories becomes imperative. Despite the importance of the problem, relatively small number of research works has been done in this area so far. In most of the works authors are paying attention to the separate aspects of FinFET testing and suggesting local solutions for each situation. For example, in [6] and [7], the authors have investigated several types of open and short defects in FinFET logic circuits and showed that an open defect on the back gate causes delay and leakage problems unique to FinFETs.

In [8] and [9], the authors have examined stuck-open faults (SOF) for FinFET-based memories and proposed two new vector strategies for increasing the possibility of SOF defects detection.

978-1-4673-7776-8/15/$31.00 ©2015 IEEE

Finally in [10], the authors examined stuck-open, stuck-on and gate oxide short defects on different number of Fins within one FinFET transistor. According to the results if this number is large enough, the defect can be modeled with stuck-open or delay faults.

However, to the best of our knowledge, there is no study conducted that pays attention to all the specifics of FinFET testing. Thus a comprehensive study was conducted to investigate the various test aspects of FinFET-based memories including the defect types, inherent fault models, efficient test algorithms and the influence of different test conditions (voltage, temperature, frequency) on fault coverage.

This paper is organized as follows. Section II gives an introduction to test methodology development flow used for embedded memories. Section III presents the defect types considered for FinFETs in the frame of the study. In Section IV, the strategy used for defect injection fault modeling and test algorithm synthesis for FinFET-based memories is outlined. Section V highlights some important experimental results obtained in the frame of the study. Finally, Section VI draws the main conclusions.

2. Test methodology development flow

The requirements for different aspects of embedded memory test and repair change from transistor technology generation to generation, which is used in memories. It is a natural process since each generation of the transistor can have structural and behavioral differences compared to the previous one. Thus the test methodology can differ among different generations. During the recent years this process was somehow stabilized since the usage of MOSFET transistor technology in the embedded memories became prevailing. The scalability of MOSFET technology allowed constantly shrinking the technology without serious impact on memory Built-in Self-Test (BIST) solutions used. The typical flow for test methodology development looks like pictured in Fig. 2. With each technology change the following major steps are completed to obtain the upgraded BIST solution:

1. *Technology Node Selection*: Each time new technological node is available it needs to be investigated in order to construct the accurate embedded test and repair solution for it.
2. *Defect Injection*: The characteristics of the arriving technology node are analyzed and based on the results new defect types are identified specific for the technology. These defects are then injected into memory in order to investigate their behavior.
3. *Fault Extraction*: As the next step, for the set of injected defects the corresponding memory faults models need to be extracted, which reflect the behavior of the defects at functional level.
4. *Test Solution Construction*: For the set of identified fault models the optimal test solution is constructed which detects the faults in the optimal period of time.
5. *BIST Solution Upgrade:* Finally the constructed test solution is integrated into the memory BIST for providing the high fault coverage.

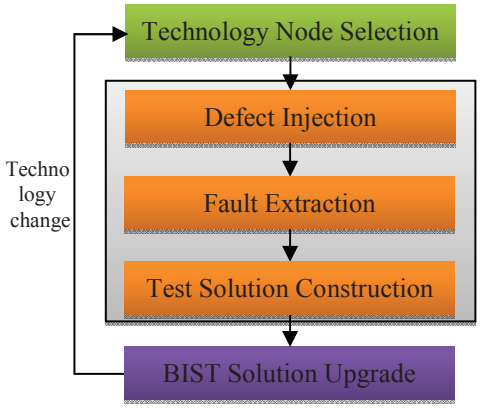

Figure 2. Test methodology development flow for embedded memories

Using this flow the set of MOSFET technology specific defects was well investigated and corresponding fault models were developed along the shrinking of technology. Nevertheless for the latest generation of MOSFET transistors, especially starting from around 65nm and down to 20nm, this flow was mainly used to define the probability of the faults occurrence since no new types of faults were being identified any more.

However the situation extremely changes with the MOSFET technology coming to its limits at 20nm. In order to cross this border new technological solutions come to the action and the established methodology need to be accustomed to them. This especially applies to FinFETs since the spatial structure of FinFET transistors paves the way for new types of defects to arise and thus leading to new fault models and possibly new test algorithms for their detection. Thus there is a need to accustom the steps of the flow (highlighted with grey box in Fig. 2), namely “Defect Injection”, “Fault Extraction” and “Test Solution Construction” for FinFET-based memories. The aim of the conducted study was to investigate the effect of the technology change from MOSFET to FinFET on each of the mentioned steps of the flow and enhance them for FinFETs. In next sections the high level overview

results of the study are presented, for which more details can be found in our previous works [11]-[13].

3. FinFET defect models

As mentioned above, the sharp differences in structures of planar MOSFET and non-planar FinFET technologies mean that the same set of defects that was considered for MOSFETs cannot be applied to FInFETs without any change. Fig. 3 shows the basic set of defect types which were considered for FinFETs in the "Defect Injection" step. This list includes defects specific to FinFETs as well as defects common for both technologies:

(a) Fin Open – Full and resistive open defects on Fin;

(b) Gate Open – Full and resistive open defects on Gate;

(c) Fin Stuck-On – Full and resistive short defects between Source and Drain;

(d) Gate-Fin Short – Full and resistive short defects between Gate and Fin;

(e) Fin-VDD/VSS Short – Full and resistive short defects between Fin and VDD or Fin and VSS.

(f) Process Variation – Variations in FinFET parameter values.

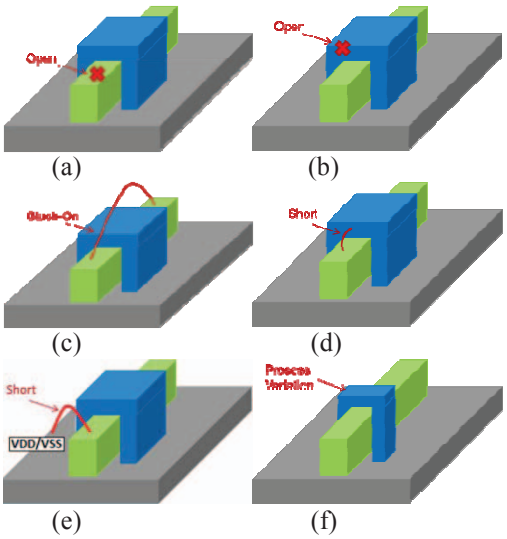

Figure 3. Defect models considered for FinFETs

Also other types of defects such as resistive/full shorts and opens placed on/between memory bit-lines and word-lines, defects of the memory array surrounding blocks (e.g. address decoder and sense amplifier) were also considered in the frame of the study in order to get the full picture.

4. Defect injection, fault modeling and test algorithm synthesis

After the set of defects going to be investigated was fixed, the next step was to inject the defects into the FinFET-based memory and model the resulting faults. For making this process more systematic and less time consuming an automatized flow was developed (see Fig. 4). It made the investigation of FinFET defects a lot faster and more effective in terms of finding new faults specific to FinFETs. As an input the flow receives the set of defects through Defect LIB and Simulation Setup containing a set of test sequences, with their test conditions (frequency, voltage, temperature), in case of resistive defect also the range of resistance magnitude. If at least of the provided test sequences detects the fault then the satisfactory Test Sequences (may be more than one) are received as an output. Otherwise, the simulation setup needs to be updated and the same process should be repeated with the new setup. Based on the received test sequences the fault models are extracted automatically. This was only a high level overview, more detailed description of the flow can be found in [11] and [12].

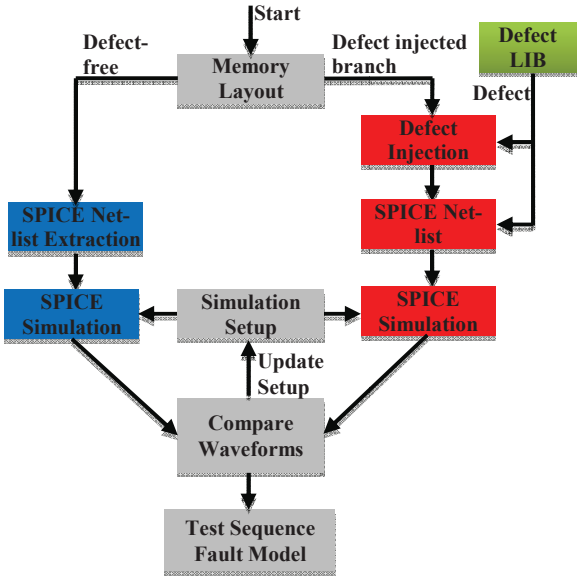

Figure 4. Defect Injection and Fault Modeling Flow

The next major step after the fault models and the corresponding test sequences are identified is the construction of a test algorithm for detection of a given set of faults. This step of the flow was also automatized to take as an input a set of Test Sequences and generate the optimal test algorithm. The advantage of this approach is that the flow becomes more generic compared to the previously existing test algorithm

generation tools (e.g., [14]-[15]) since there is no dependency on fault types. Besides it becomes more efficient since the output test sequences of the described flow become direct inputs for the algorithm generation flow and all these happens automatically without any need for human intervention. Also it is important to note that our experiments show that if the given Test Sequences have minimal lengths in terms of detecting the given defects/fault models, then Test Algorithm Generator will synthesize minimal test algorithms.

5. Experimental results

The proposed flow was validated on several FinFET-based memories obtained from different foundries. The results of the performed huge number of SPICE simulations proved the viability of the described solution and led to some interesting results summarized in [11], [12]. Some of the most important statements derived are listed below:

- FinFET-based memories are more prone to dynamic faults than planar-based memories.
- FinFET-based memories are more stable to process variation faults.
- Static single-cell and coupling faults are typical for both FinFET- and planar-based memories.

The study was continued even further to investigate the impact of different test conditions including temperature, voltage and frequency on fault coverage of the proposed test solutions. As a result, number of recommendations were worked out which can help to make the test solutions for FinFETs even more effective (please refer to [12] and [13] for more details).

6. Conclusions

This paper presents the overview of the extended study the aim of which was to investigate FinFET-based memories and accustom the typical test methodology construction flow for them. Each of the steps in the flow was investigated in detail and the required enhancements are outlined which need to be applied. For this purpose a new strategy was proposed which helps to make the flow more systematized and automatized in order to reduce the time and efforts necessary for modeling FinFET-specific faults and synthesizing test algorithms for their detection.

The results of experiments done for several real-life FinFET-based memories prove the usefulness of the flow and reveal some interesting characteristics of FinFET-based memories. In particular the experiments showed that FinFET-based memories compared with planar-based memories are more prone to dynamic faults and are more stable to process variation faults.

In future works more attention is going to be paid to investigation of debug and diagnosis aspects of FinFET-based memories.

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