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Memory Physical Aware Multi-Level Fault Diagnosis Flow

SAMVEL SHOUKOURIAN, GURGEN HARUTYUNYAN, SUREN MARTIROSYAN, YERVANT ZORIAN

IEEE Transactions on Emerging Topics in Computing 2020 700-711

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Fault Awareness for Memory BIST Architecture Shaped by Multidimensional Prediction Mechanism

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IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2019 562-575

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Experimental study on Hamming and Hsiao Codes in the Context of Embedded Applications

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Automated Flow for Test Pattern Creation for IPs in SoC

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An Efficient Testing Methodology for Embedded Flash Memories

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Overview study on fault modeling and test methodology development for FinFET-based memories.

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Testing Electronic Memories Based on Fault and Test Algorithm Periodicity

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FINFET-BASED MEMORY TESTING USING MULTIPLE READ OPERATIONS

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DETECTION OF ADDRESS ERRORS IN MEMORY DEVICES USING MULTI-SEGMENT ERROR DETECTION CODES

Samvel Shoukourian, Gurgen Harutyunyan, Hayk Grigoryan, Grigor Tshagharyan, Yervant Zorian
